IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR U.S. LETTERS PATENT

Title:

CIRCUIT AND ASSOCIATED METHODOLOGY

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CIRCUIT AND ASSOCIATED METHODOLOGY

DESCRIPTION OF RELATED ART

[0001] In logic circuitry, the term "gate" refers to a circuit that implements a basic digital logic function. Examples of gates include AND, OR, inverter, and multiplex (mux) circuits. A domino mux gate circuit is commonly used to evaluate logic input signals, depending on the phase of an input clock cycle.

SUMMARY

[0002] In accordance with an embodiment, a circuit for evaluating logic level input signals is provided. The circuit includes a pre-charge node and a clock evaluate node coupled to cause charging of the pre-charge node in response to the logic level of the clock evaluate node. The circuit further includes an output node coupled to the pre-charge node through inverter logic circuitry and a plurality of logic input signal nodes configured to receive logic level input signals. The circuit further includes multiple pull-down stacks interconnected with the pre-charge node, each pull-down stack including an interstitial node and coupled to discharge the pre-charge node to ground in response to logic level input signals. The interstitial node of each pull-down stack couples to an interstitial pre-charger, which further couples to deliver charge to the interstitial node in response to the logic level of the clock evaluate node. The interstitial node additionally couples to an interstitial discharger, which is gated to ground and coupled to discharge the interstitial node to ground in response to the logic level of the clock evaluate node.

[0003] In accordance with another embodiment, a method of interstitial pre-discharge in a circuit with multiple pull-down stacks is provided. The method includes providing the circuit, which includes a pre-charge node and a clock evaluate node coupled to the pre-charge node and operable to receive a clock evaluate input cycle. Multiple pull-down stacks each including an interstitial node interconnect the pre-charge node and ground. The interstitial node of each pull-down stack couples to an interstitial discharger device, which is gated to ground. The method further includes operating the circuit in a pre-charge phase of the clock evaluate input cycle, including pre-charging the pre-charge node and the interstitial nodes, and keeping the devices in the pull-down stacks and the interstitial dischargers in a high impedance state. The method additionally includes operating the circuit in an evaluate

phase of the clock cycle, including discharging the pre-charge node to ground through a pull-down stack, and discharging the interstitial node to ground through the interstitial discharger device to preclude a charge share event.

[0004] In accordance with yet another embodiment, a circuit is provided. The circuit includes means for storing a pre-charge and means for causing the pre-charge. The circuit further includes means for output coupled to the means for storing the pre-charge, means for receiving logic level input signals, and means for discharging to ground the means for storing the pre-charge in response to the logic level input signals. The circuit further includes the means for discharging coupled to means for pre-charging in response to the means for causing the pre-charge, and the means for discharging coupled to means for pre-discharging in response to the means for causing the pre-charge.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] FIGURE 1 shows a circuit embodiment including a domino type muxing structure logic gate with the addition of four Field Effect Transistors (FETs);

[0006] FIGURE 2 shows a domino mux gate circuit similar to that of FIGURE 1 but without the interstitial pre-charge p-type FETs (PFETs);

[0007] FIGURE 3 shows a simulation timing diagram of operation of the circuit of FIGURE 2, which demonstrates a charge share event;

[0008] FIGURE 4 shows a circuit similar to that of FIGURE 1 but without predischarge and gating FETS, demonstrating another type of charge sharing;

[0009] FIGURE 5 shows simulation timing diagrams of the circuit of FIGURE 4;

[0010] FIGURE 6 shows simulation timing diagrams for the circuit of FIGURE 1 with the same inputs as shown in FIGURE 5;

[0011] FIGURE 7 shows a circuit similar to that of FIGURE 1, but without gating FETs;

[0012] FIGURE 8 shows simulation timing diagrams for the circuit of FIGURE 7, which include a transient drive fight;

[0013] FIGURE 9 shows a circuit including a full keeper, i.e. both PFET and NFET holders on a pre-charge node; and

[0014] FIGURE 10 is a flow diagram depicting an operational sequence of a domino gate circuit with multiple pull-down stacks using a gated interstitial pre-discharge, in accordance with circuit embodiments herein.

DETAILED DESCRIPTION

[0015] FIGURE 1 shows circuit embodiment 100 including a domino-type multiplexing (muxing) structure logic gate with the addition of four Field Effect Transistors (FETs) 17-2, 15-4, 17-1 and 15-3. The term "gate" refers to a circuit that implements a basic digital logic function. Examples of gates include AND, OR, inverter, and mux circuits. The term "domino logic" is commonly interchangeably referred to as dynamic logic.

[0016] Other FETs in circuit 100 include FETs 11, 12-1, 12-2, 13. P-type FET (PFET) 13 is referred to as a "holder" or "keeper." Its purpose is to prevent the charge on pre-charge node 102 from leaking away through drain-to-source leakage during the evaluate clock phase. For example, if signal input nodes 105-1 and 105-2 are at ground, pre-charge node 102 is pre-charged to supply voltage VDD (logic 1), and clock evaluate node 101 transitioned to VDD, then pre-charge node 102 should remain at logic 1, but since the voltage on pre-charge node 102 is being held only by the charge stored on the capacitance of pre-charge node 102, in the absence of PFET 13 the charge will eventually leak away through the two high resistance paths to ground through n-type FET (NFET) pull-down stacks containing NFETS 14-1 to 14-6 and 15-1, 15-2.

[0017] An interstitial node is a term used in the art to describe a node between two FETs that are in series with one another. The purpose of PFETs 12-1 and 12-2 is to charge the capacitance on interstitial nodes 104-1 and 104-4 to VDD (logic 1) during the pre-charge phase of the clock signal 101. These PFETs are referred to as interstitial pre-chargers, because they serve to charge the capacitance of interstitial nodes of the circuit during the pre-charge phase of evaluate clock 101. The reason for pre-charging the interstitial nodes of the circuit is to avoid "charge sharing" between the interstitial nodes and pre-charge node 102

during the evaluate phase of evaluate clock 101. Other interstitial nodes in circuit 100 include nodes 104-2, 104-3, 104-5, 104-6, 108-1, and 108-2.

[0018] FIGURE 2 shows domino mux gate circuit 200, similar to circuit 100 of FIGURE 1 but without interstitial pre-charge p-type FETs (PFETs) 12-1 and 12-2. Circuit 200 has two modes of operation, namely pre-charge and evaluate. When "evaluate" clock signal 101 is at a low voltage (logic 0), the circuit is in pre-charge mode. During this phase of the clock cycle, PFET 11 forms a conductive channel, and pre-charge node 102 charges to supply voltage VDD (logic 1) through the channel of PFET 11. Pre-charge node 102 is coupled with output node 103 through an inverter logic subcircuit containing PFET 16-2 and NFET 16-1. By the end of the pre-charge phase, pre-charge node 102 reaches a high voltage at or near VDD, PFET 16-2 has no conductive channel, and n-type FET (NFET) 16-1 has formed a conductive channel. Thus output node 103 pre-discharges to a low voltage through the conductive channel of NFET 16-1. At the end of the pre-charge phase, the circuit is enabled to evaluate input logic signals.

[0019] When clock signal evaluate 101 is at a high voltage (logic 1), mux circuit 200 is said to be in an evaluate mode. During this mode of operation, logical evaluations are performed. This time period is referred to as the evaluate phase of the clock cycle. During the evaluate phase, if signal input nodes 105-1, 106 and 107-1 rise to a logic 1 level, then a conductive path is formed from pre-charge node 102 to the low voltage supply ground through NFETs 14-1, 14-2, 14-3 and 15-1, respectively, and pre-charge node 102 discharges to ground (logic 0). Similarly, during the evaluate phase of the clock cycle, if signal inputs 105-2, 106 and 107-2 rise to a logic 1 level, then a conductive path is formed from pre-charge node 102 to ground through NFETs 14-4, 14-5, 14-6 and 15-2, respectively, and pre-charge node 102 discharges to ground (logic 0). If neither of these two conditions occurs, pre-charge node 102 remains at or near VDD (logic 1). If pre-charge node 102 discharges to ground, then output node 103 will charge to VDD through PFET 16-2. Otherwise, output node 103 will remain at ground.

[0020] FIGURE 3 shows a simulation timing diagram of operation of circuit 200 of FIGURE 2, which demonstrates a charge share event. For the simulations, the vertical axis is voltage and the horizontal axis is time. Most important are the general waveforms and how they relate to one another qualitatively in time. Less important are the absolute time

scale on the x-axis and raw y-axis values. Circuit embodiments 100, 200, 400, 700, and corresponding timing diagrams herein relate to circuit topology and not to any specific implementation. The simulation waveforms illustrate general behavior via the operation of specific implementations, because they provide an easy way to capture timing relationships between important signals. The waveform diagrams are labeled only with zero volts and VDD on the y-axis and are labeled with time on the x-axis in picoseconds, but the scales can be interpreted as completely arbitrary, so long as the waveforms maintain consistent timing relationships with one another.

[0021] In the simulation depicted in FIGURE 3, clock evaluate node 101 transitions to voltage V-101 equal to logic 1 in waveform 301, pre-charge node 102 is pre-charged to voltage V-102 equal to logic 1 in waveform 351, voltage V-104-1 is at logic 0 in waveform 321, voltage V-105-2 and voltage V-107-1 are at logic 0 in waveforms 331 and 341 respectively, and voltage V-105-1 transitions from logic 0 to logic 1 in waveform 311. Then current flows through the channel of NFET 14-1 from pre-charge node 102 to interstitial node 104-1. Charge (Q=CV) that was stored on the capacitance of pre-charge node 102 is shared with the capacitance of interstitial node 104-1. Because of conservation of charge, the voltage on pre-charge node 102 is seen to droop after the charge share event. The droop is described approximately by the equation:

$$V\text{-}102\_final = (C\text{-}102 * V\text{-}102\_initial)/(C\text{-}102 + C\text{-}105\text{-}1)$$

[0022] Charge sharing is undesirable, because logically pre-charge node 102 is intended to stay at logic 1, but the charge share causes V-102 to droop (point 352 in waveform 351) enough that V-103 rises (Point 362 in waveform 361). If V-103 rises to a voltage above the sensitivity threshold of downstream logic, the signal could be interpreted as a logic 1, whereas it is intended to be a logic 0.

[0023] FIGURE 4 shows circuit 400 similar to circuit 100 of FIGURE 1 but without pre-discharge and gating FETS 15-3, 15-4, 17-1, and 17-2, demonstrating another type of charge sharing. FIGURE 5 shows simulation timing diagrams of circuit 400: V-105-1=logic 1, V-107-1=logic 1, V-106=logic 1, in respective waveforms 521, 531, and 541. Clock evaluate V-101 transitions to logic 1 in waveform 301, V-107-2=logic 0 (not shown) and V-105-2 goes high in waveform 551. Then the charge that was stored on the capacitance of nodes 104-4 and 104-5 shares with the capacitance of pre-charge node 102, i.e., current

flows from nodes 104-5 and 104-4 to node 102 as depicted in waveform 561. This causes the voltage of pre-charge node 102 to rise (Point 572 in waveform 571). A rise in voltage V-102 on pre-charge node 102 causes voltage V-103 on output node 103 to drop (point 582 in waveform 581). This is an unintended behavior, since the voltage on output node 103 should stay at logic 1 until the next pre-charge phase.

[0024] This charge sharing problem is addressed by the embodiments as illustrated, for example, in circuit 100 depicted in FIGURE 1. In accordance with the embodiments, whenever pre-charge node 102 is pulled low, interstitial nodes 104-4 and 104-1 are discharged, precluding the possibility of charge sharing with pre-charge node 102 when pre-charge node 102 is low. FIGURE 6 shows simulation timing diagrams of circuit 100 of FIGURE 1 with the same inputs as in FIGURE 5, namely V-107-1=logic 1 in timing diagram 541, V-106=logic 1 in timing diagram 531, evaluate V-101=logic 1 in timing diagram 301, V-107-2=logic 0 (not shown) and V-105-1 going high in timing diagram 521. With the inclusion of interstitial dischargers 17-2 and 17-1, the capacitances of interstitial nodes 104-1 and 104-4 are discharged in timing diagrams 661, 671 prior to respective input signals V-105-1 in timing diagram 521 or V-105-2 in timing diagram 551 going high. Therefore, there is no charge to couple onto pre-charge node 102, and no discontinuity in V-102 on pre-charge node 102 is observed (point 682 in timing diagram 681). Consequently, signal V-103 on output node 103 in timing diagram 691 remains at logic 1 and does not droop. In FIGURES 1, 2, and 7, for purposes of illustrating the circuit topology, interstitial node 104-1 is shown in two places once between FETs 14-1 and 14-2 and again in series with interstitial discharger 17-1. In the circuits, these occurrences both actually lie on a single node. Likewise, in FIGURES 1, 2, and 7, the two appearances of interstitial node 104-4 both actually lie on a single node.

[0025] Interstitial dischargers 17-2 and 17-1, are gated by respective evaluation FETs 15-4 and 15-3, precluding any drive fight between pre-charge FETs and interstitial dischargers 17-2 and 17-1. A drive fight occurs at a particular node in a circuit when two different drivers try to drive some common node that they share to two different voltages. "Driver" here can be from as simple as a single transistor up to a complex circuit. Drive fight is a term well known in the art.

[0026] A drive fight occurs when there is a channel-connected (low resistance) path from VDD to ground. FIGURE 7 shows circuit 700 similar to circuit 100, but without FETs 15-3 and 15-4. FIGURE 8 shows simulation timing diagrams of circuit 700, which include a transient drive fight (Point 863 in waveform 861). All signal amplitudes in FIGURE 8 represent voltage on a scale from zero to VDD, except signal i-108-2, which represents current waveform 861 into the drain of interstitial discharger NFET 17-2. In the simulation, pre-charge node V-102 transitions to logic 0 in waveform 681, input V-105-2=logic 1 in waveform 851, and evaluate clock 101 transitions from 1 to 0 in waveform 301. Initially, both FET 14-4 and interstitial discharger 17-2 have conductive channels. As V-102 rises (pre-charges), current flows through FET 14-4 and interstitial discharger 17-2 to ground. In the absence of evaluation FET 15-4, the drive fight is a transient event that lasts until output node 103 goes low in waveform 691 and shuts off interstitial discharger 17-2. Discharging of the interstitial node through interstitial discharger 17-2 due to circuit evaluation is demonstrated at Point 862 in waveform 861.

[0027] Alternative techniques to those of circuit 100 that have been employed include:

- FIGURE 9 shows circuit 900, including a full keeper, i.e. both PFET 13 and NFET 93 holders on pre-charge node 102. However, NFET holder 93 needs to be quite large, i.e. the NFET gate width needs to be quite large, to significantly reduce the size of the unintended and unwanted voltage discontinuity on pre-charge node 102. This adversely increases the capacitive loading on pre-charge node 102, thus increasing the evaluation time of pre-charge node 102. Evaluation time is the delay from the time an input, e.g. 105-1 or 105-2, rises until output node 103 rises. Increased capacitive loading also adversely increases pre-charge time, because the pre-charge FET 12-1 and 12-2 must fight against NFET keeper 93 to pre-charge node 102 high. Pre-charge time is the time delay from the falling edge of evaluate clock V-101 to the rising edge of pre-charge signal V-102.

- Increasing the trip point of output inverter subcircuit including PFET 16-2 and NFET 16-1. This subcircuit implements the logical function of inversion. The trip point of the output inverter is defined as the voltage on node 102

required to drive the output to that same voltage. The greater the width of PFET 16-2, the higher the trip point of the inverter, because of the relatively lower effective resistance of the wider PFET channel. This higher trip point adversely increases susceptibility to noise and charge sharing on pre-charge node 102 when node 102 is high.

[0028] The embodiments solve the problem of charge sharing of positive charge from interstitial nodes 104-1 and 104-2 to pre-charge node 102 of a domino gate circuit, for example circuit 100, during the evaluation phase, preventing an undesired rising voltage discontinuity on pre-charge node 102 that could otherwise produce an undesired voltage droop on output node 103.

[0029] FIGURE 10 is a flow diagram depicting operational sequence 1000 of a domino gate circuit, for example circuit 100, with multiple pull-down stacks using a gated interstitial pre-discharge, in accordance with circuit embodiments herein. In operation 1001, domino gate circuit 100 is provided, which includes multiple pull-down stacks, clock evaluate input node 101, multiple logic signal input nodes, for example signal input nodes 105-1, 105-2, 106, 107-1, and 107-2. Circuit 100 additionally includes pre-charge node 102, output node 103, and interstitial nodes, for example interstitial nodes 104-1 and 104-4 connecting adjacent FETs within the multiple pull-down stacks. Interstitial nodes 104-1 and 104-4 are individually interconnected with respective interstitial pre-chargers 12-1 and 12-2 and with respective interstitial dischargers 17-1 and 17-2, which are gated to ground through respective evaluation FETs 15-3 and 15-4.

[0030] In an example pre-charge phase, as depicted in operation 1002, evaluate input node 101 and signal input nodes 105-2, 107-2 are at logic 0, and signal input nodes 105-1, 106, and 107-1 are all held at logic 1 (i.e., VDD) in operation 1003. This causes pre-charge node 102 and interstitial nodes 104-1 and 104-4 to be pre-charged to logic 1 through pre-chargers 12-1 and 12-2 and through PFET 11 respectively in operation 1004. Output node 103 consequently discharges to logic 0 in operation 1005. Channels to ground through the pull-down stacks and through the evaluation FETs are all held in a high impedance (low conductance) condition by connecting their respective gates to evaluate input node 101 in operation 1006.

[0031] In an example evaluate phase, as depicted in operation 1007, evaluate input node 101 transitions from logic 0 to logic 1 in operation 1008, causing channels to ground through pull-down stacks and evaluation FETs to become conductive in operation 1009. Pre-charge node 102 then discharges to logic 0 (ground) through one of the pull-down stacks in operation 1010, causing output node 103 to charge to logic 1 in operation 1010. Concurrently PFET 11 and pre-chargers 12-1 and 12-2 transition to high impedance in operation 1011, stopping pre-charge of pre-charge node 102 and the interstitial nodes in operation 1012, and interstitial dischargers 17-1 and 17-2 transition to high conductance in operation 1013, causing the interstitial nodes to discharge to logic level 0 (ground) in operation 1014, which in operation 1015 precludes charge sharing that could otherwise adversely introduce a voltage droop on output node 103.